those along the edge or edges of the sub assembly (claim 1) or the printed circuit board (claim 8).

Claim Rejections - 35 USC § 102

Claims 1-4, and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Beilstein, Jr. et al. (reference cited by applicant).

As best understood to claim 1, Beilstein discloses an electronic sub assembly (30-figure 2, column 4, line 22) as shown in figures 2-5 comprising

a circuitized laminated substrate (module 32, column 4, line 23) having top and bottom surfaces (19, 17-figure 2, column 4, line 29), and at least one edge surface (21; 33, column 4, line 29, and column 6, line 37) between said top and bottom surfaces,

one or more active or passive devices (42, 38-figure 2) mounted on at least one of the top and bottom surfaces (19, 17),

a conductive lead (37-figure 3) embedded in the substrate (32) electrically connected to another active or passive device (70-figure 3) mounted on said at least one edge surface (33-figure 3), the conductive lead also electrically connected to at least one device on the top or bottom surface.

Beilstein does disclose and describe metallized interconnections between components of a multichip package. In addition to the customary metallized contacts on the planar top and bottom surfaces, the patent discusses the use of at least one end surface having a metallization pattern thereon. However, contrary to the contention of the examiner, the reference does not clearly disclose a "conductive lead also electrically connected to at least one device on the top or bottom surface." The conductive lead 37 that the examiner highlights is no more than a connect pad in the form of a solder bump (Col. 6, lines 35-36) that is on the end surface of the laminate, not "embedded in the substrate..." as specified in applicants' claim 1.

Claim 1 as now amended can now be further distinguished from the structure of Beilstein in that the edge surface of the claimed sub assembly is beveled (i.e. not at right angles) to the planar surfaces. Again, this feature is not disclosed nor suggested by Beilstein. Yet it can yield a significant increase in the exposed edge surface area that is available for contact with active or passive devices or with other sub assemblies.

Prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. Jamesbury Corp. v. Litton Indus. Products, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); Atlas Powder Co. v. du Pont, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); American Hospital Supply v. Travenol Labs, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984). Applicants respectfully submit that the cited prior art does not include each and every element of claim 1 as filed. Furthermore, claim 1 as amended is even further removed from the scope of the Beilstein reference. Accordingly, the rejection of claim 1 should be withdrawn.

As to claim 2, Beilstein discloses the electronic sub assembly (30) as shown in figures 2-5 wherein each of the active or passive devices is selected from the group including chips (38, 42).

Claim 2 denotes the types of devices that are adapted to be mounted to the top, the bottom or the edge surfaces of the sub assembly. This limitation further describes what is contemplated as an active or passive device useful within the framework of the invention as claimed by amended claim 1. Applicants respectfully submit that claim 1 is not anticipated by Beilstein. Accordingly, claim 2 should be deemed to be patentably distinct over this same reference.

As to claim 3, Beilstein discloses the electronic sub assembly as shown in figures 2-5 further including an electrically conductive via (via 40, column 4, line 51, and via 44, column 5, line 2) extending into the substrate from each device (38, 42) on the top or bottom surface (19, 17) into contact with a conductive lead connected to an edge mounted device.

Claim 3 is rejected on the basis that Beilstein shows a conductive via extending from a device on the top or bottom surface into contact with a conductive lead connected to an edge mounted device. As previously noted, such is not the case. There is no such disclosure in Beilstein. In fact, the examiner has taken the word "via" as it appears in line 50 of column 4 and in line 2 of column 5 of Beilstein out of context. The patent uses the word "via" at these two locations in the specification as a propositional substitute for the phrase "by means of". The word is not being used as a noun at these two locations to refer to a conductive passageway through the laminate. Accordingly, the rejection of claim 3 is erroneously predicated on a misconstruction of the language in the prior art and should be withdrawn.

As to claim 4, Beilstein discloses the electronic sub assembly (30) as shown in figures 2-5 wherein the laminated substrate is selected from the group comprising: a single or multiple laminates of a ceramic module and a conductive layer.

Claim 4 depends from independent claim 1 and should be considered as allowable for the same reasons as the claim from which it depends.

Newly submitted claim 27 depends from claim 1 and, for the same reasons as claim 1, should be deemed to be allowable. This new claim specifies an edge angle of between 30°and 60°. This limitation derives support in the specification at page 6, lines 11 and 12 of the specification, and more focused support at page 11, lines 13

and 14, which states: "To create more space on the edge 20 of the core 10, the edge can be beveled at an angle of less than 90°, e.g. between 30° and 60°."

As best understood to claim 8, Beilstein discloses a printed circuit board (32) as shown in figures 2-5 having two spaced apart, generally parallel surfaces comprising a top surface (19) and a bottom surface (17), an edge surface (21; 33) between said top and bottom surfaces, a plurality of conductive leads (37-figure 3) embedded in the circuit board (30) parallel to the top and bottom surfaces (see figure 4-5) and terminating in one or more connection points along the edge surface (33), an active or passive device (70) mounted on said edge surface and electrically joined through at least one of said connection points to at least one of the conductive leads, and at least another active or passive devices (38, 42) mounted on the top or bottom surface electrically joined to the edge mounted device.

Contrary to the contention of the examiner, the Beilstein reference does not clearly disclose a "plurality of conductive leads embedded in the PCB terminating in one or more connection points along the edge surface" as noted in claim 8. The conductive lead 37 that the examiner highlights is a connect pad in the form of a solder bump (Col. 6, lines 35-36) that is on the end surface of the laminate. It is not "embedded in the circuit board..." as specified in applicants' claim 8. Furthermore, Beilstein does not show the devices mounted on the planar surfaces being electrically joined to the edge mounted devices. Therefore, claim 8 should be deemed to be allowable.

Claim 8 as now amended can be further distinguished from the structure of Beilstein in that the edge surface of the claimed PCB is beveled (i.e. not at right angles) to the planar surfaces. Again, this feature is not disclosed nor suggested by Beilstein. Yet it can increase in the amount of edge surface area that is available for attachment to active or passive devices and to other sub assemblies.

As previously noted, prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. (see citations above). Applicants respectfully submit that the cited prior art does not include each and every element of claim 8, either as filed or as amended. Accordingly, the examiner should withdraw the rejection of claim 8, and allow the same.

As to claim 9, Beilstein discloses the printed circuit board (32) further including a via (36) on the top or bottom surface, and coupled to a top or bottom mounted device (see an interconnection of figure 2), said via extending into the substrate into contact with a conductive lead connected to said edge mounted device.

The PCB of claim 8 is deemed to be novel and patentable for the reasons stated above. Likewise, dependent claim 9, describing additional features should be considered to be patentable as well.

As to claim 10, Beilstein discloses the printed circuit board (32) wherein each said another active or passive device is selected from the group including chips.

Claim 10 depends from claim 8 and should be deemed to be allowable for the same reasons as claim 2 *supra*.

Newly submitted claim 28 depends from claim 8 and, for the same reasons as recited in connection with claim 8, should be deemed to be allowable. As previously noted, page 11, lines 13 and 14 of the specification support this limitation.

Applicants are providing clean and marked up versions of the claims, as well as of the specification paragraphs previously noted.

Applicants respectfully submit that the independent claims 1 and 8 as now amended clearly differentiate over the teachings of Beilstein and should be allowed. Accordingly, the examiner is respectfully requested to reconsider the rejection and to withdraw the rejection.

Respectfully submitted,

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